Hierarchical Graph Coloring Register Allocation in LLVM

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“Register Allocation via Hierarchical Graph Coloring”
David Callahan and Brian Koblenz, PLDI 1991

• Graph coloring register allocation
  • construct & color an interference graph
  • optimal coloring is NP complete

• Callahan-Koblenz (CK) allocator
  • hierarchy of tiles that represent loops and conditional control flow to guide allocation and spilling decisions
Implementation in LLVM

- Original prototype developed in Microsoft Phoenix
  - 10 years of testing and tuning
  - used on several targets: Arm32, AArch64, x86, x64, PPC, EDGE
  - 70k LOCs / 80 files (cpp/h/inl)

- Surgically removed and converted to C++ then rewritten to use LLVM APIs and IR
  - lib/CodeGen/RegAllocTiled.cpp that inherent from RegAllocBase
  - lib/CodeGen/TiledAlloc/* contains allocator sources

- Current implementation uses one tile for entire function with point spilling (T0)
- As of today all our benchmarks compile and run with new allocator
  - mibench, bulletphysics, parsec, spec, parboil, ...
  - performance within 5% of greedy without any advanced features

- Coming soon...
  - cost model / edge profile support
  - rematerialization
  - multiple tiles
  - spilling heuristics
  - other targets (x64, AArch64)

- Releasing soon! Get in touch if you would like to collaborate!