enabling heterogeneous hardware acceleration using novel programming and scheduling models

**PROJECT TOPICS & WORKING PACKAGES**

- **Automatic Program Analysis and Semi-Automatic Parallelization**
  - C / C++ / Fortran
  - Performance modeling implements determination of runtimes by static analysis with LLVM and the automated estimation of object memory footprints alongside with their data-directions

- **Checkerpointing Detection and Insertion**
  - Intermediate Code
  - We instrument the code with the LLVM Functions, BasicBlock, Instruction manipulation to insert the user space scheduler calls

- **Performance Modeling and Generic Components**
  - Performance modeling implements determination of runtimes by static analysis with LLVM and the automated estimation of object memory footprints alongside with their data-directions

- **C / C++ / FORTRAN Application**
  - Program Analysis
  - Pre-Processing
  - Loop Optimization Parallelization
  - Code Generation
  - Checkpointing
  - Performance Model

- **Resource Management and Scheduling**
  - OS / Scheduler

- **Runtime Layer**
  - CPU
  - GPU
  - FPGA

- **Application**
  - Thermodynamics
  - Particle Dynamics
  - Aeroacoustics
  - Genome Analysis
  - Map Reduce Framework

- **THE ENHANCE CONSORTIUM**

  - **TWT GmbH Science & Innovation**
  - **Fraunhofer SCAI**
  - **ZIB**
  - **openpba member**

- **PROJECT DURATION**
  - April 2011 – September 2013

- **Support the application developer by a tool-chain with semi-automatic parallelization capabilities**
- **Optimization of loops by transforming memory access patterns**
- **Hardware aware transformations and optimization approach**

- **Project targets a system platform with Multi-Core, GPU & FPGA processing devices**
- **OS should schedule tasks on different processing devices depending on available resources**
- **Kernel metadata support decision making**

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