MLIR GEMM Code Generation

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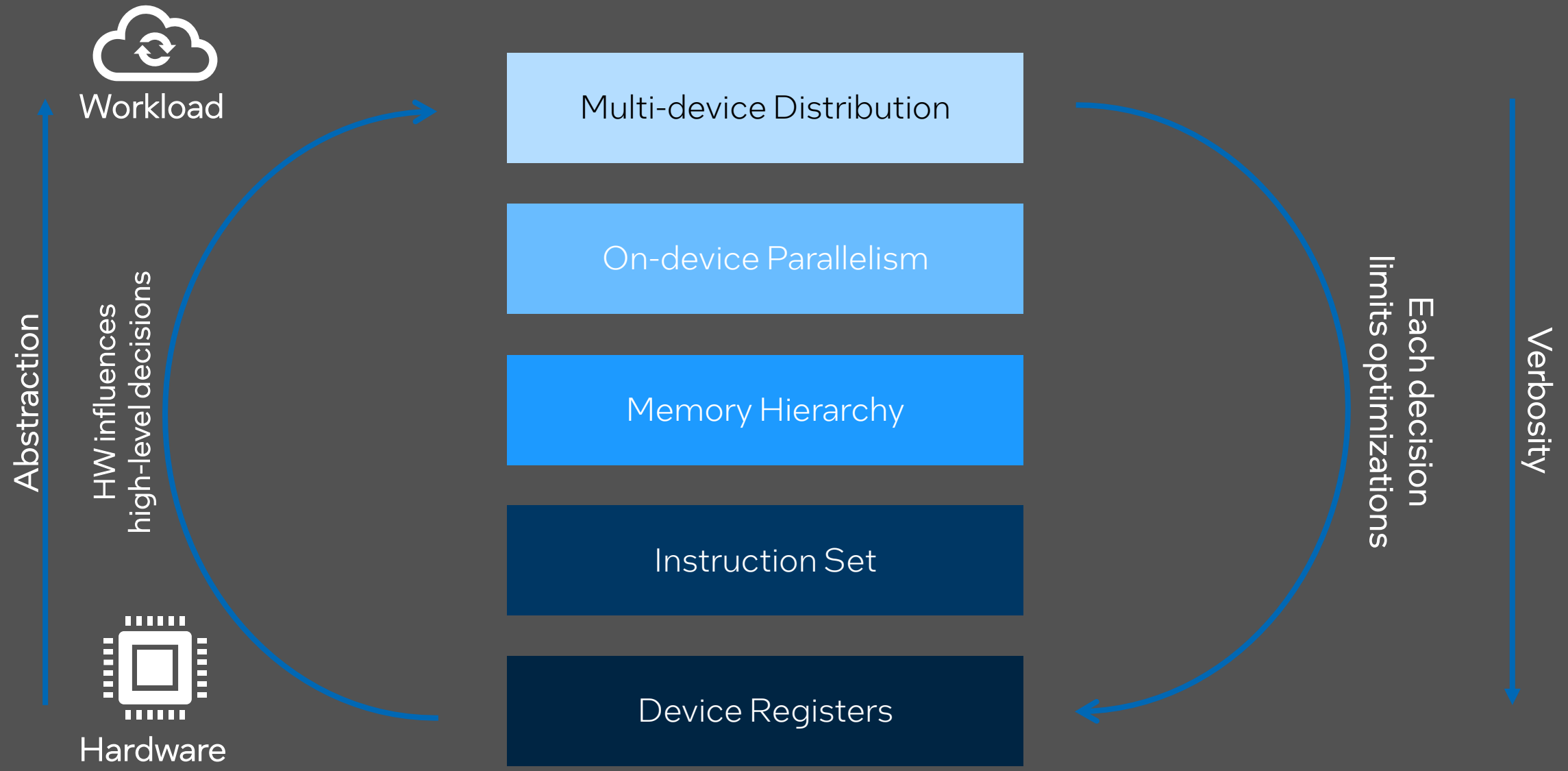
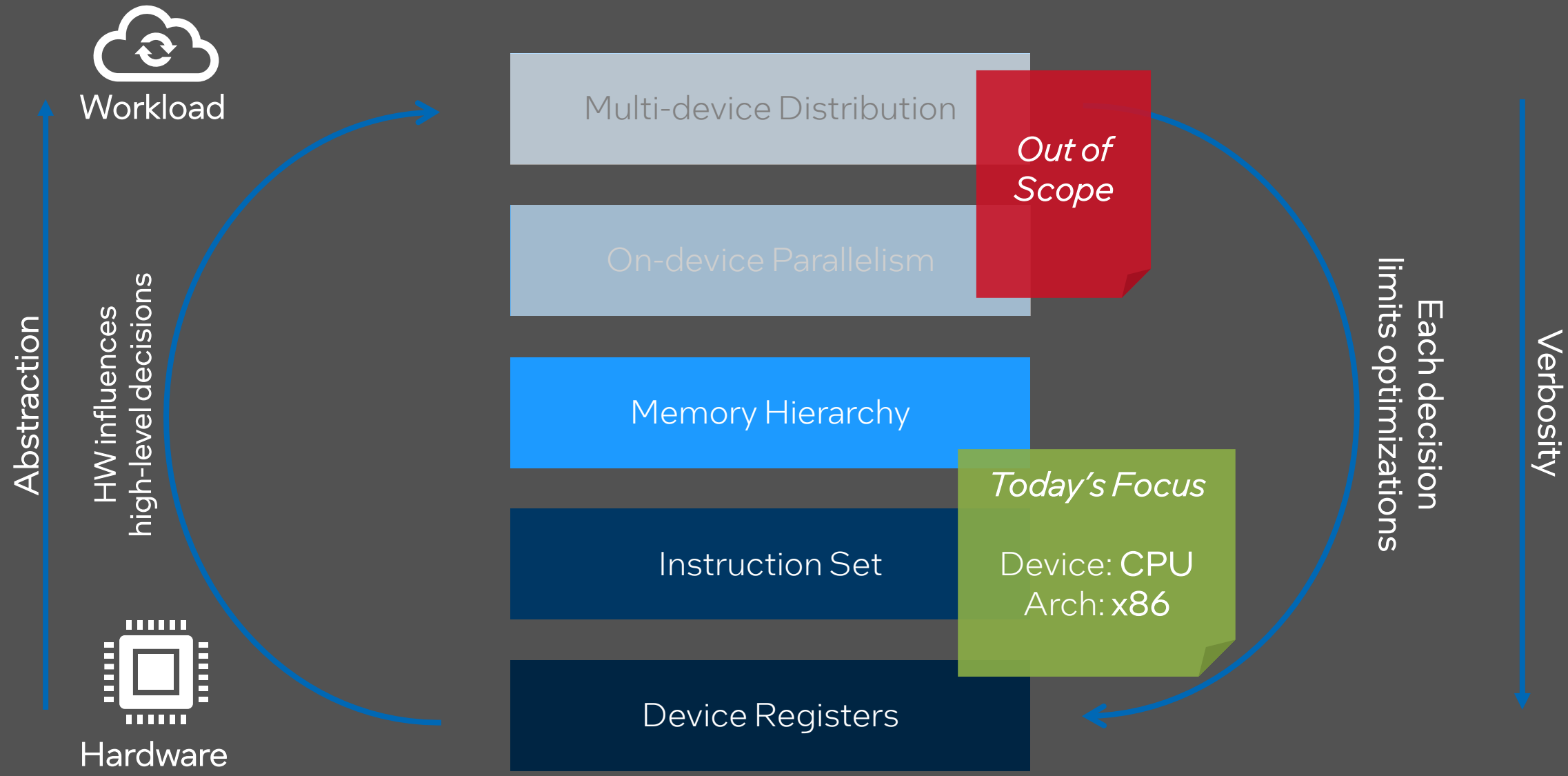
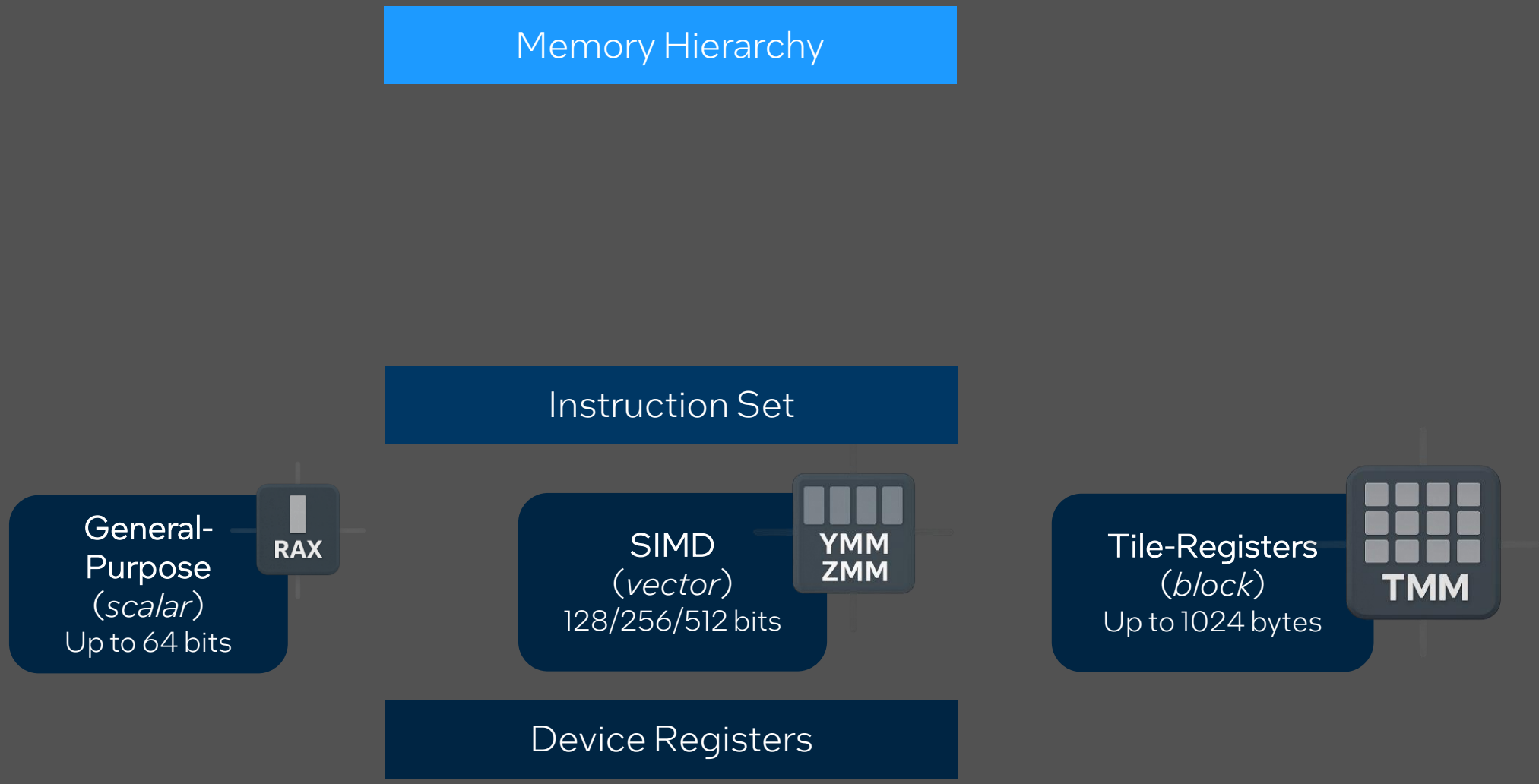
Hardware-Software Feedback Loop



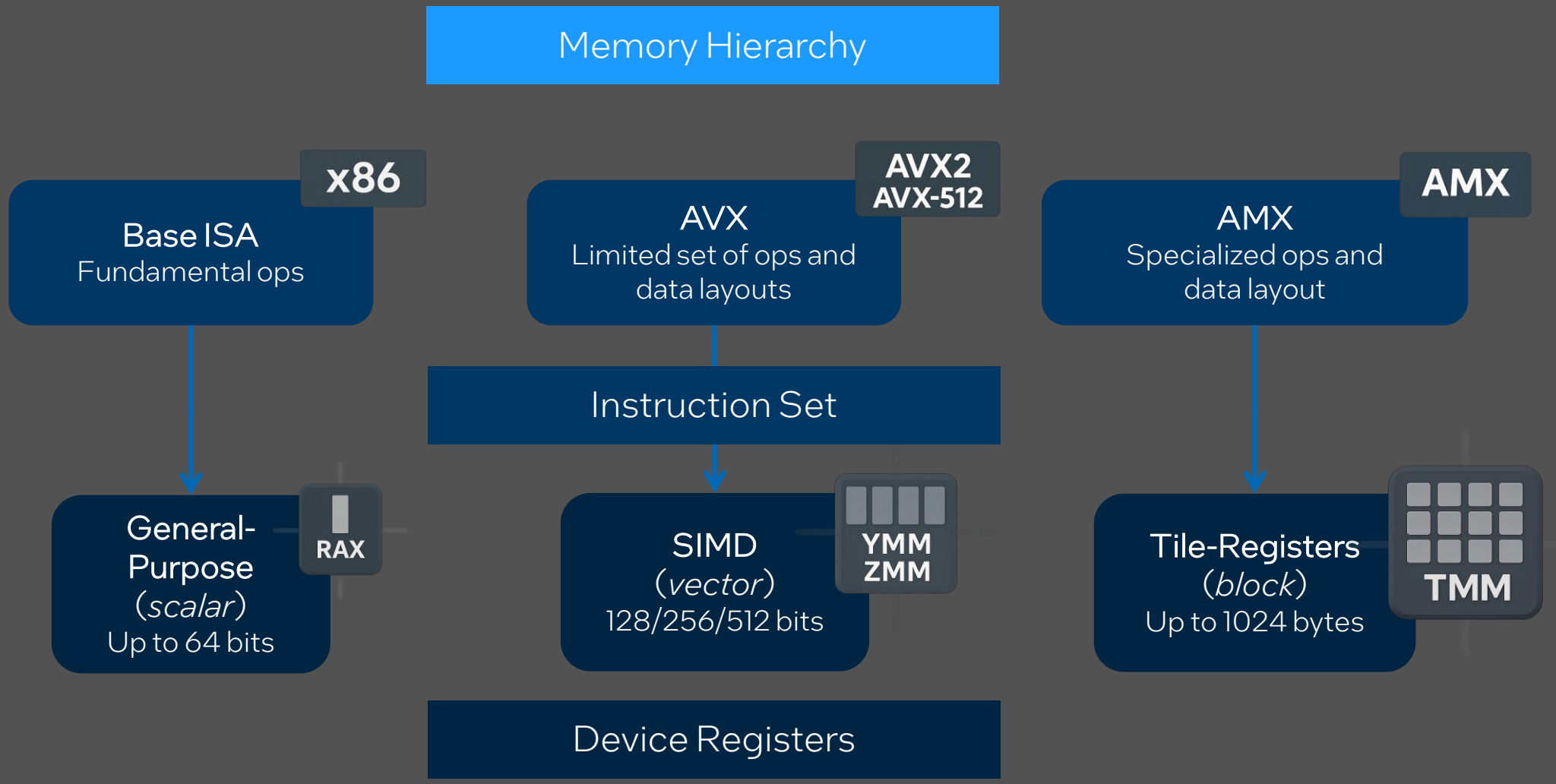
Hardware-Software Feedback Loop



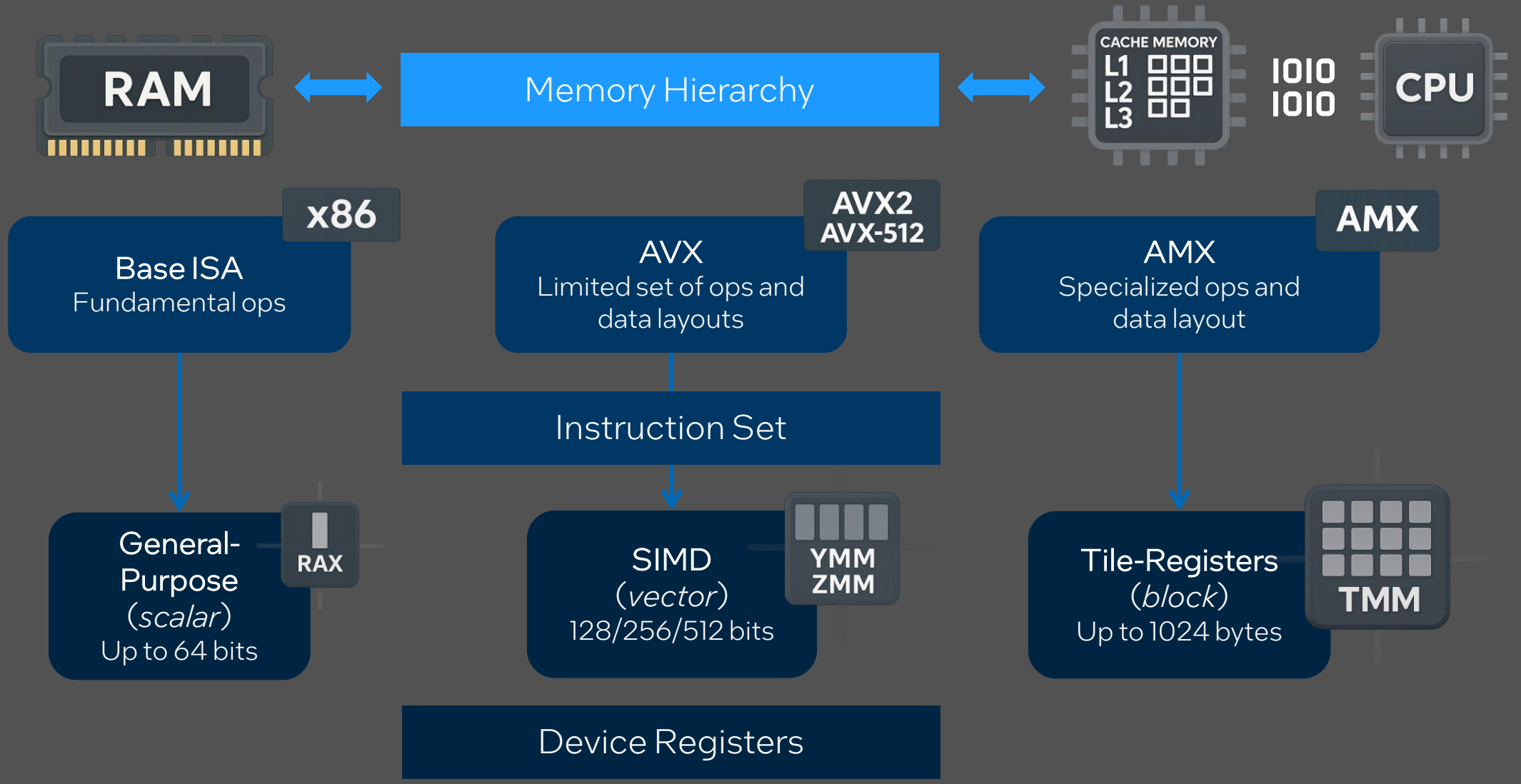
Hardware Building Blocks



Hardware Building Blocks



Hardware Building Blocks



MLIR ➡️ Memory

Memory Hierarchy

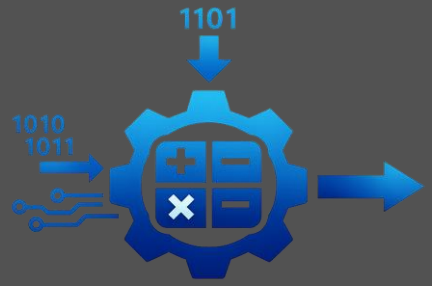
Matrix Multiply:

```
C += A * B

A <M x K>
B <K x N>
C <M x N>
```

B

A



C

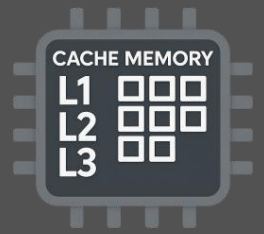
linalg.matmul

MLIR ➡️ Memory

Matrix Multiply:
`C += A * B`

`A <M x K>`
`B <K x N>`
`C <M x N>`

Tile
Upper
Bound



Memory Hierarchy

Tile

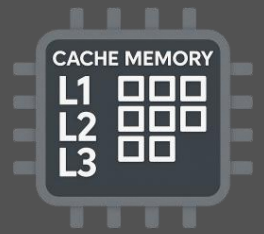
Block Pack

Fuse

Tile
Lower
Bound

MLIR ➡️ Memory

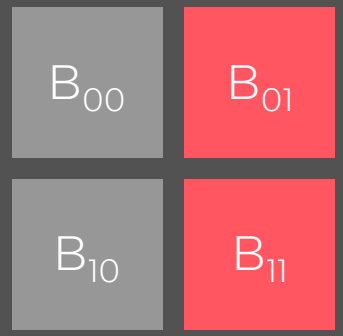
Tile
Upper
Bound

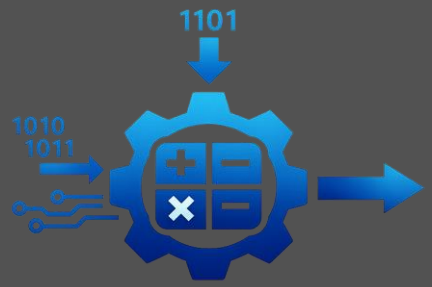


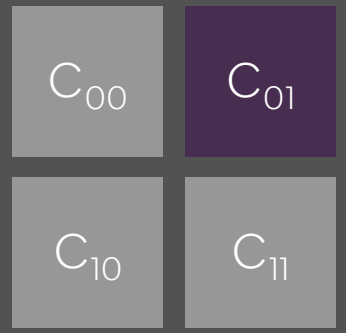
Memory Hierarchy

Matrix Multiply:
`C += A * B`

`A <Mb x K>`
`B <K x Nb>`
`C <Mb x Nb>`







linalg.matmul

Tile
Block Pack
Fuse

Tile
Lower
Bound

MLIR ➡️ Registers

Instruction Set

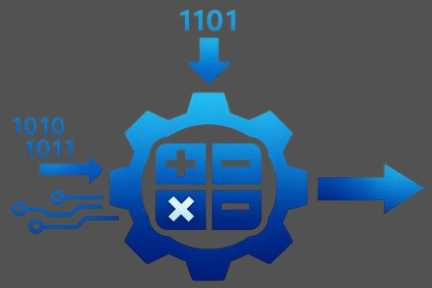
MICRO KERNEL

Matrix Multiply:

```
C += A * B

A <Mb x K>
B <K x Nb>
C <Mb x Nb>
```

B_{K1}



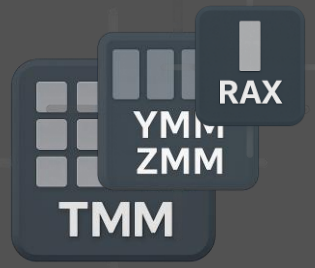
A_{0K}

C_{01}

linalg.matmul

MLIR ➡️ Registers

Tile
Upper
Bound

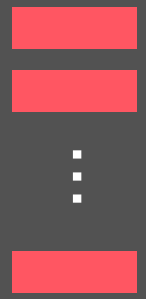


Instruction Set

Matrix Multiply:

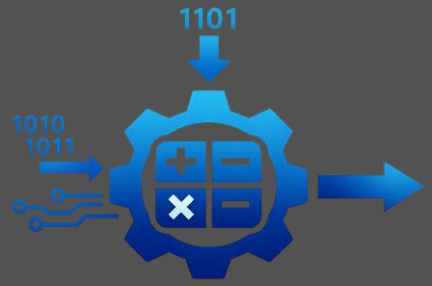
```
C += A * B

A <mr x k>
B <k x nr>
C <mb x nr>
```



$B_{[0:k:K]0}$

$A_{1[0:k:K]}$



linalg.matmul

C_{00}	C_{01}
C_{10}	C_{11}
C_{20}	C_{21}

Tile

Loop
Interchange

Loop Peel

Tile
Lower
Bound

MLIR ➡️ Instructions

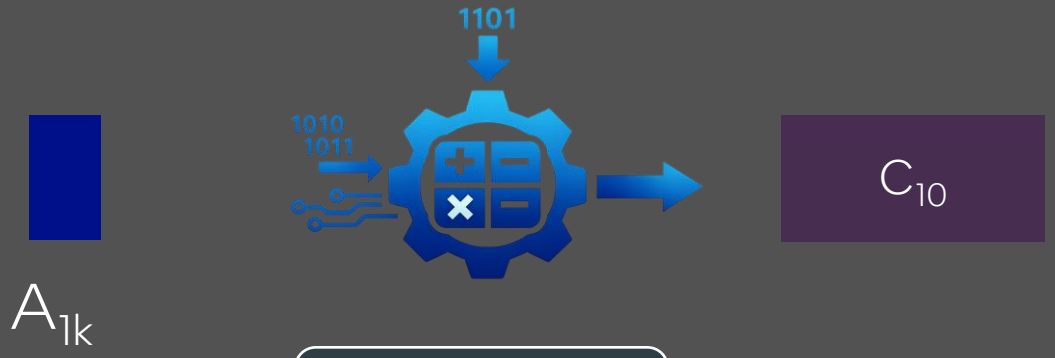
Instruction Set

Matrix Multiply:
`C += A * B`

AVX2
AVX-512

```
A <8 x 2>  BF16
B <2 x 32> BF16
C <8 x 32> F32
```

B_{k0}



linalg.matmul

MLIR ➡️ Instructions

Tile Target

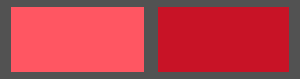
x86
AVX-512
AMX

Instruction Set

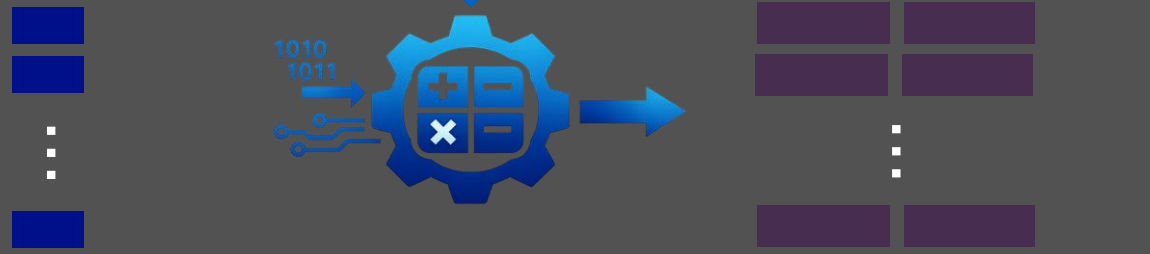
Matrix Multiply:
`C += A * B`

AVX2
AVX-512

```
A <1 x 2>   BF16
B <2 x 16>  BF16
C <1 x 16>  F32
```



$B_{k[0:16:32]}$



$A_{[0:1:8]k}$

linalg.matmul

$C_{[0:1:8][0:16:32]}$

Tile

Loop Unroll

x86
AVX-512

MLIR ➡️ Instructions

Tile Target

x86
AVX-512
AMX

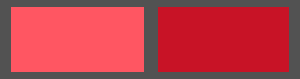
Instruction Set

NANO KERNEL

Matrix Multiply:
`C += A * B`

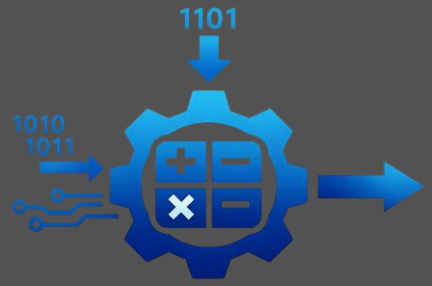
AVX2
AVX-512

```
A <1 x 2>   BF16
B <2 x 16>  BF16
C <1 x 16>  F32
```

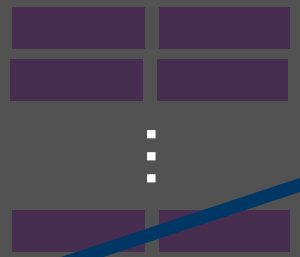


$B_{k[0:16:32]}$

$A_{[0:1:8]k}$



vector.contract



$C_{[0:1:8][0:16:32]}$

Tile

Loop Unroll

Vectorize

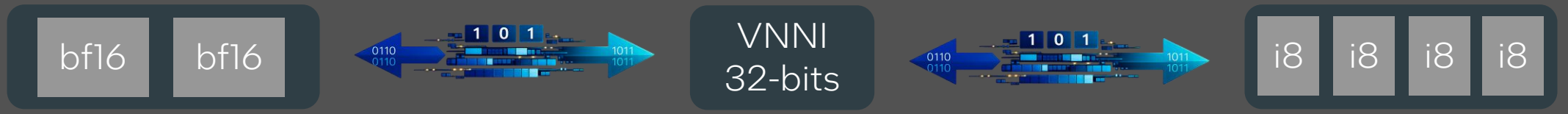
Loop Hoist

x86
AVX-512

VNNI Data Layout

AVX2
AVX-512

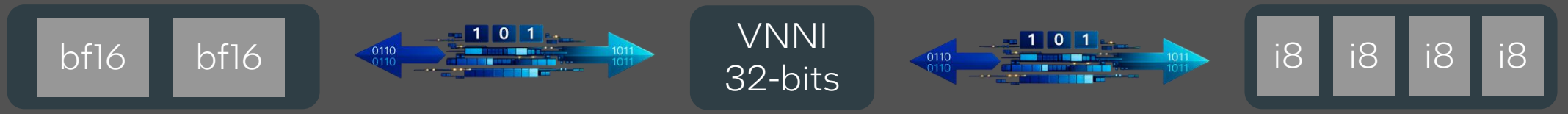
AMX



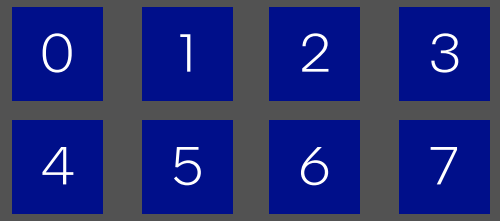
VNNI Data Layout

AVX2
AVX-512

AMX



A <2 x 4> BF16



A <2 x (2 x 2)> BF16

VNNI Data Layout

AVX2
AVX-512

AMX

bf16 | bf16

VNNI
32-bits

i8 | i8 | i8 | i8

A <2 x 4> BF16

0	1	2	3
4	5	6	7

A <2 x (2 x 2)> BF16

0	1	2	3
4	5	6	7

B <4 x 2> BF16

0	1
4	5
2	3
6	7

B <(2) x 2 x (2)> BF16

0	4	1	5
2	6	3	7

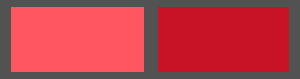
MLIR ➡️ AVX-512 BF16

AVX-512 Instruction Set

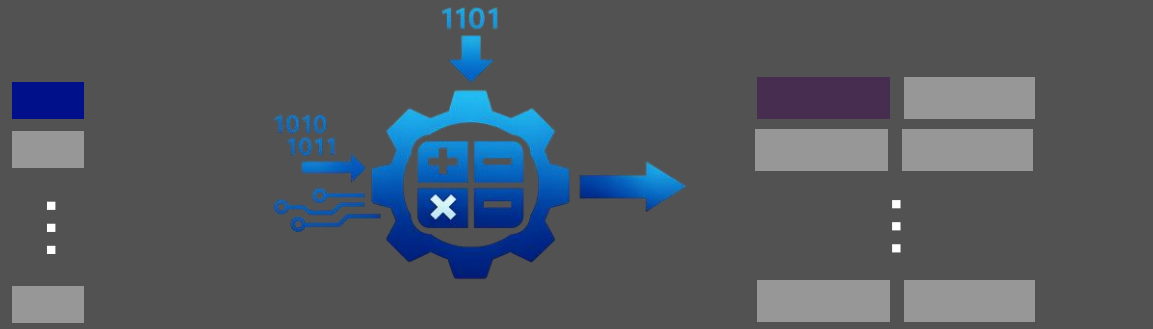
Matrix Multiply:

```
C += A * B
```

```
A <1 x 2>   BF16
B <2 x 16>  BF16
C <1 x 16>  F32
```

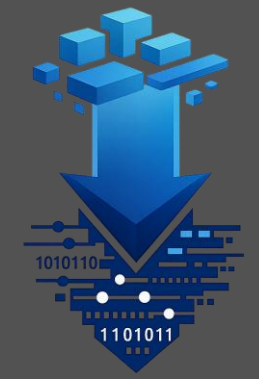


$B_{k[0:16:32]}$



$A_{[0:1:8]k}$

$C_{[0:1:8][0:16:32]}$



x86

AVX-512

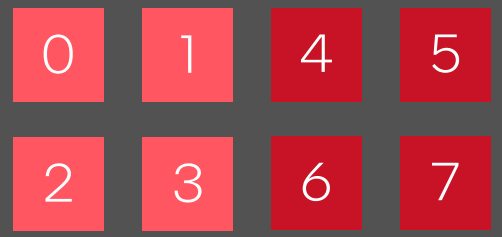
MLIR ➡️ AVX-512 BF16

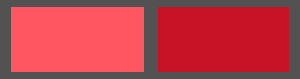
AVX-512 Instruction Set

Matrix Multiply:
`C += A * B`

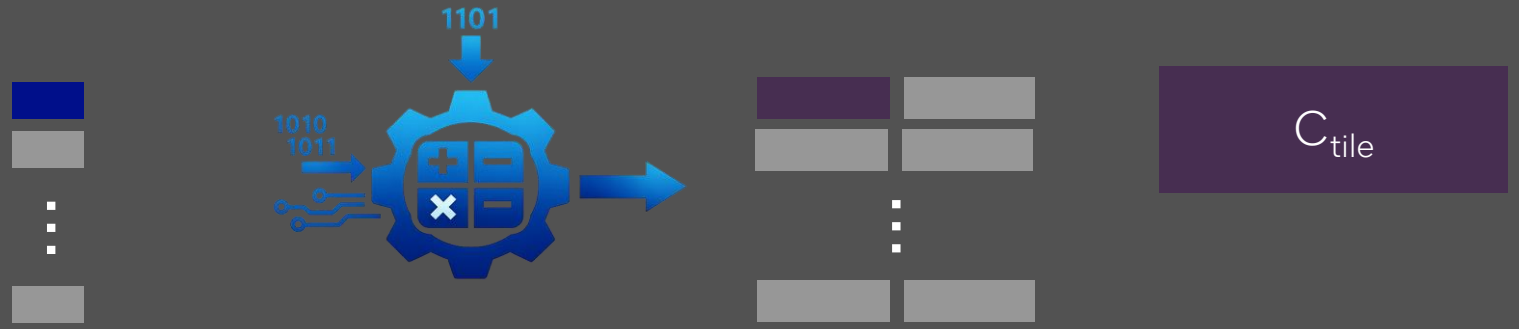
```
A <1 x 2>  BF16
B <2 x 16> BF16
C <1 x 16> F32
```

`2 x B <2 x 2> BF16`





$B_{k[0:16:32]}$



$A_{[0:1:8]k}$

vector.contract

$C_{[0:1:8][0:16:32]}$

C_{tile}

`A <1 x 2> BF16`

NANO KERNEL

x86

AVX-512

MLIR ➡️ AVX-512 BF16

AVX-512 Instruction Set

A <1 x 2> BF16

2 x B <2 x 2> BF16

x86 Patterns

x86

AVX-512

MLIR ➡️ AVX-512 BF16

AVX-512 Instruction Set

A <1 x 2> BF16

x86 vector.bitcast

x86 vector.broadcast

2 x B <2 x 2> BF16

AVX-512 vector.shuffle

NANO KERNEL

x86 Patterns

x86

AVX-512

MLIR ➡️ AVX-512 BF16

AVX-512 Instruction Set

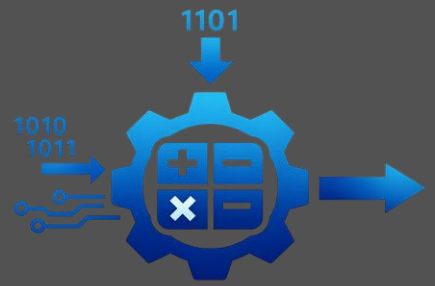
A <1 x 2> BF16

x86 vector.bitcast

x86 vector.broadcast

2 x B <2 x 2> BF16

AVX-512 vector.shuffle



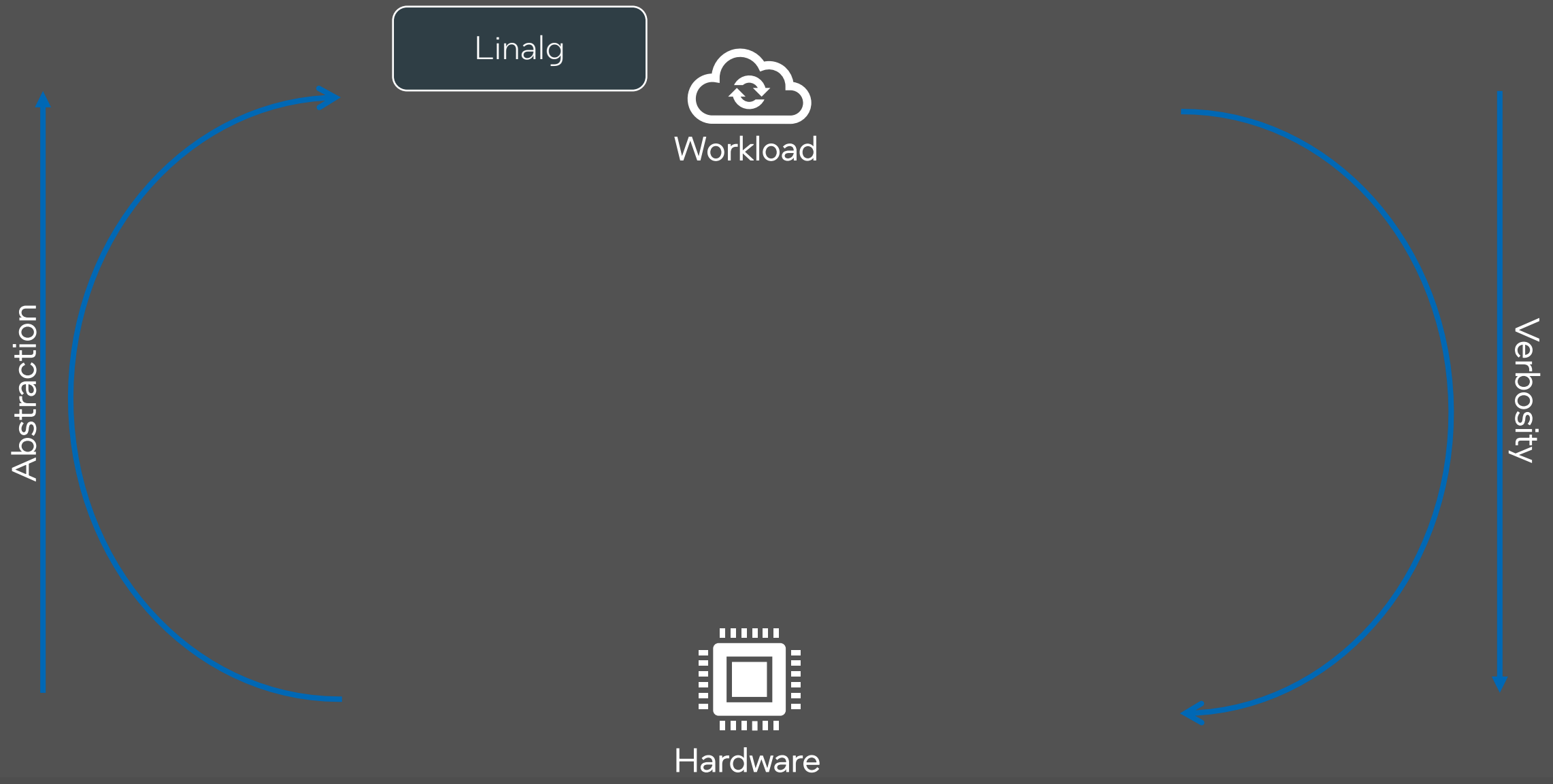
C_{tile}

AVX-512 x86.avx512.dot

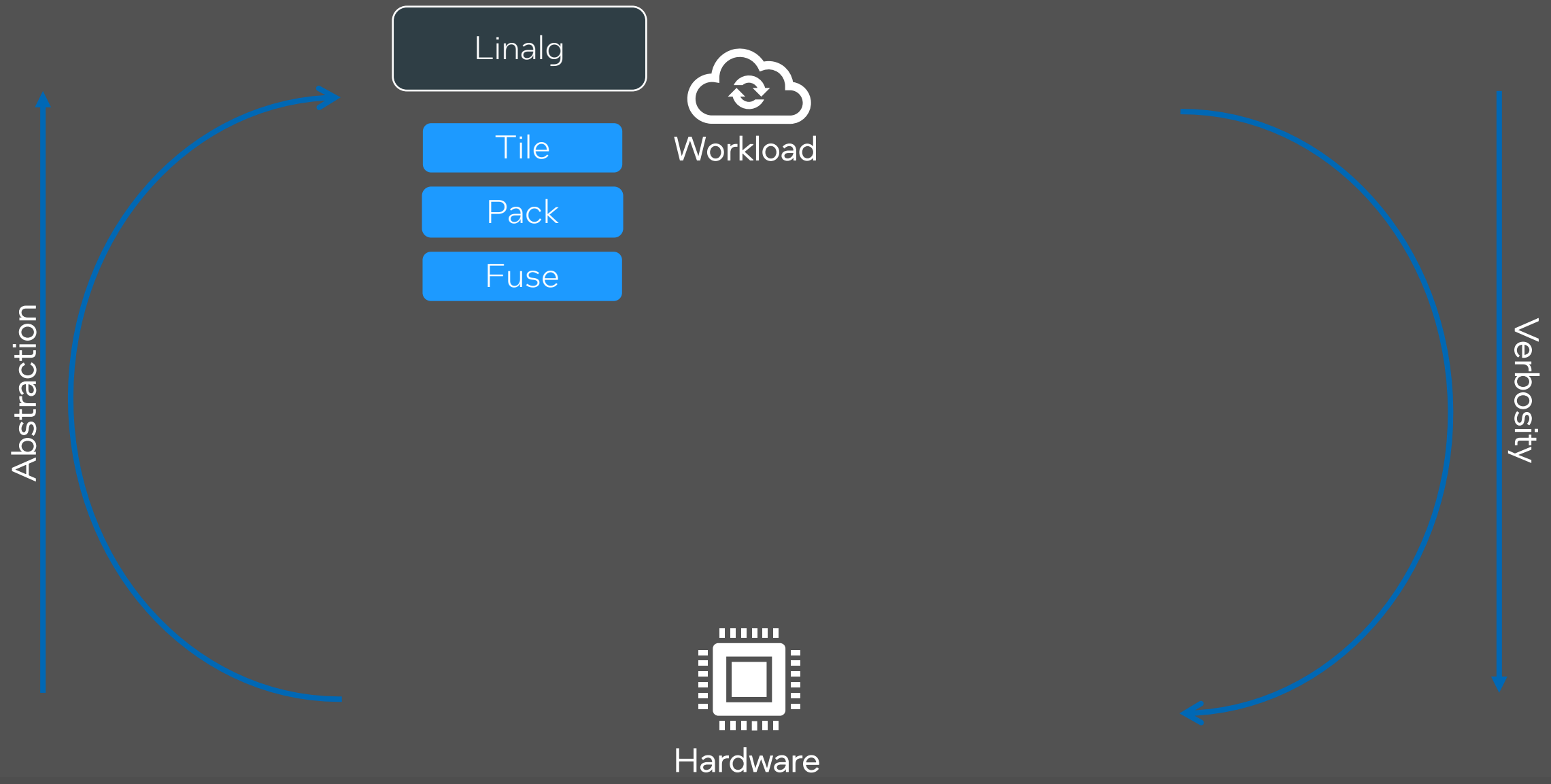
x86 Patterns

x86
AVX-512

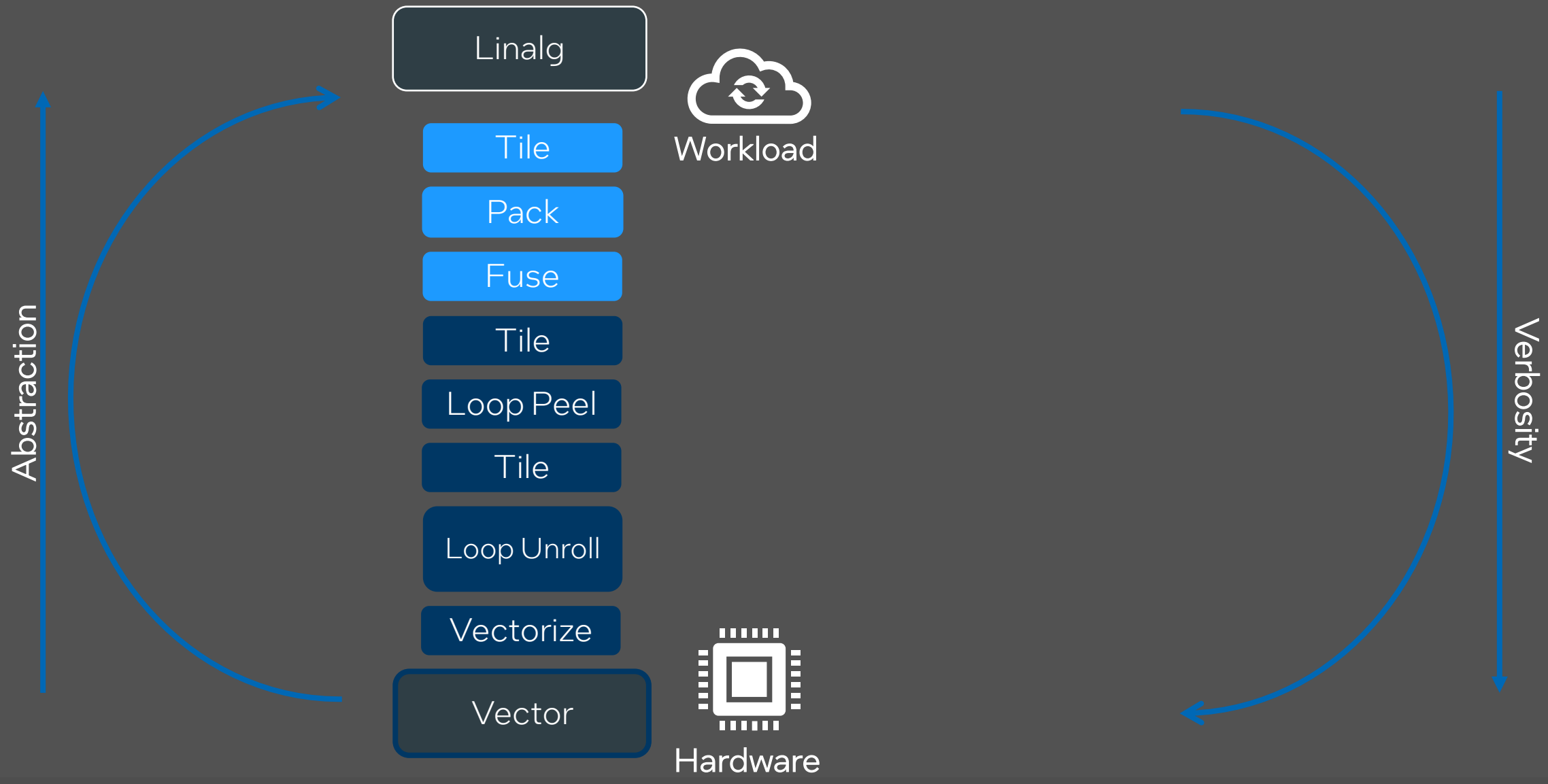
MLIR ➡️ x86



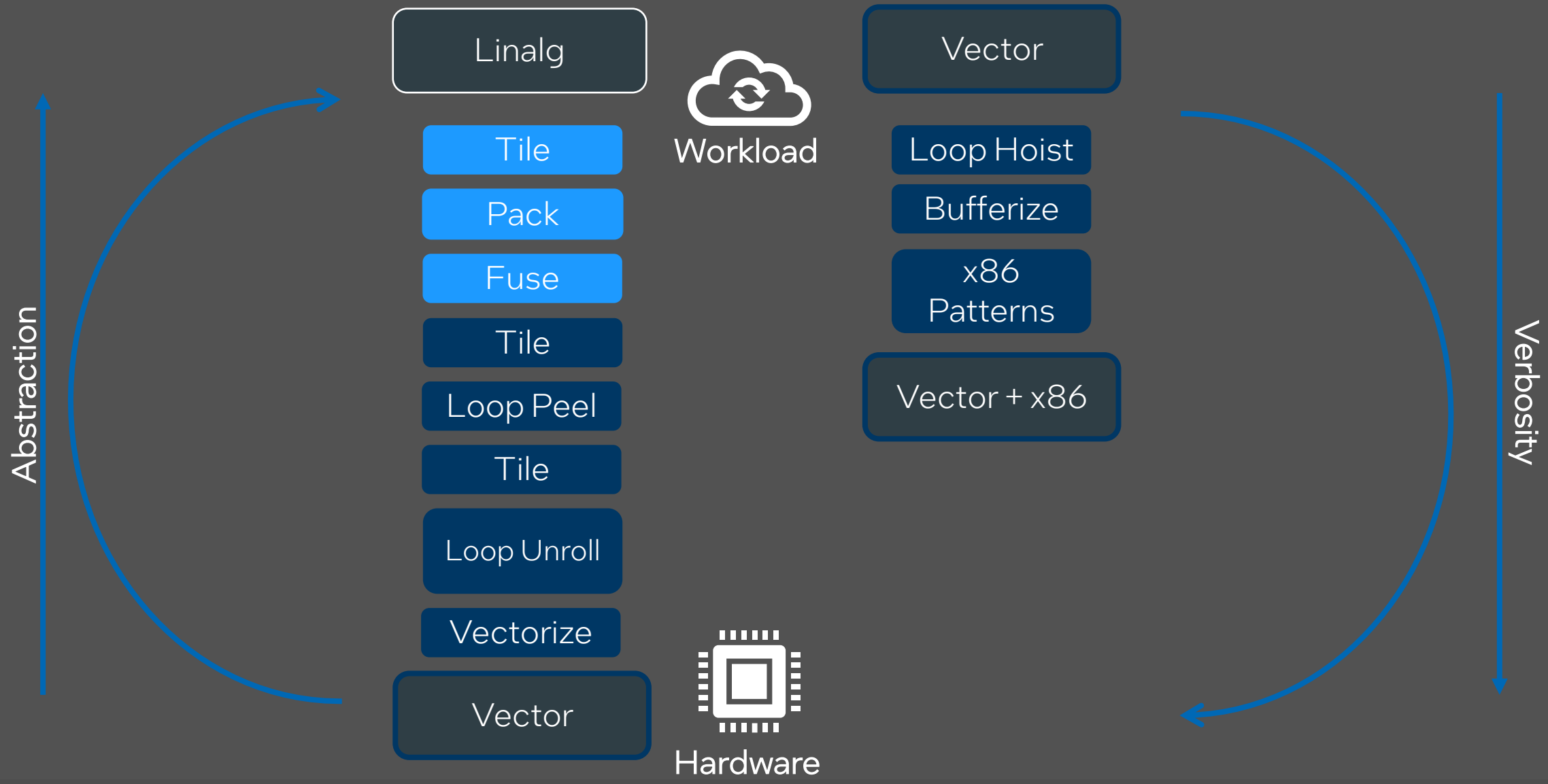
MLIR ➡️ x86


Linalg
Tile
Pack
Fuse
Workload
Abstraction
Verbosity
Hardware

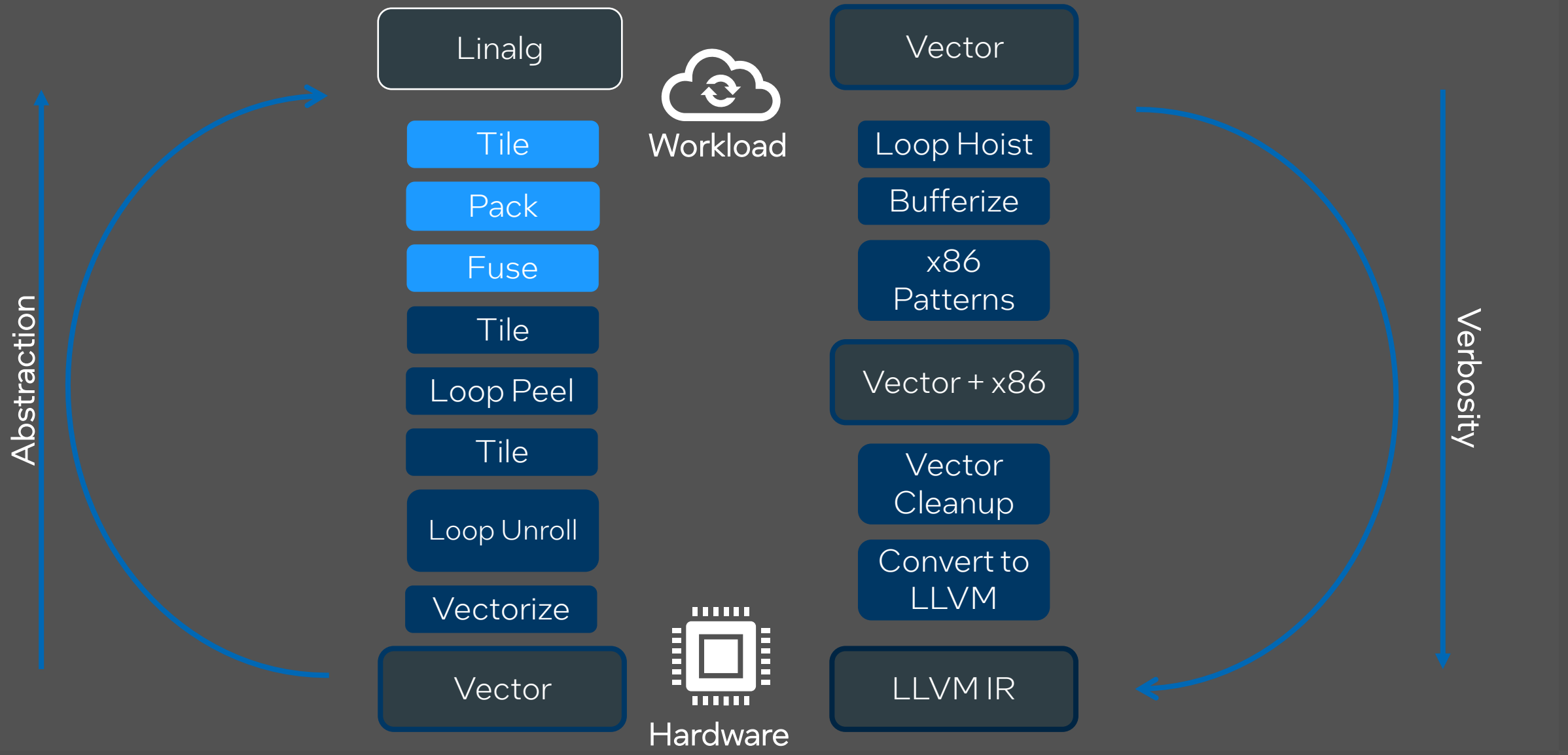
MLIR ➡️ x86


Linalg
Tile
Pack
Fuse
Tile
Loop Peel
Tile
Loop Unroll
Vectorize
Vector
Workload
Hardware
Abstraction
Verbosity

MLIR ➡️ x86


Linalg
Tile
Pack
Fuse
Tile
Loop Peel
Tile
Loop Unroll
Vectorize
Vector
Workload
Hardware
Vector
Loop Hoist
Bufferize
x86 Patterns
Vector + x86
Abstraction
Verbosity

MLIR ➡️ x86


Linalg
Tile
Pack
Fuse
Tile
Loop Peel
Tile
Loop Unroll
Vectorize
Vector
Workload
Hardware
Vector
Loop Hoist
Bufferize
x86 Patterns
Vector + x86
Vector Cleanup
Convert to LLVM
LLVM IR
Abstraction
Verbosity

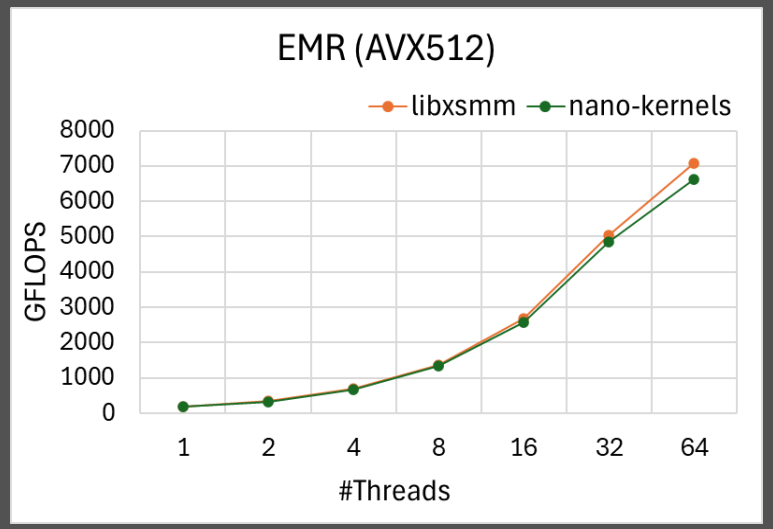
Benchmarks - Setup

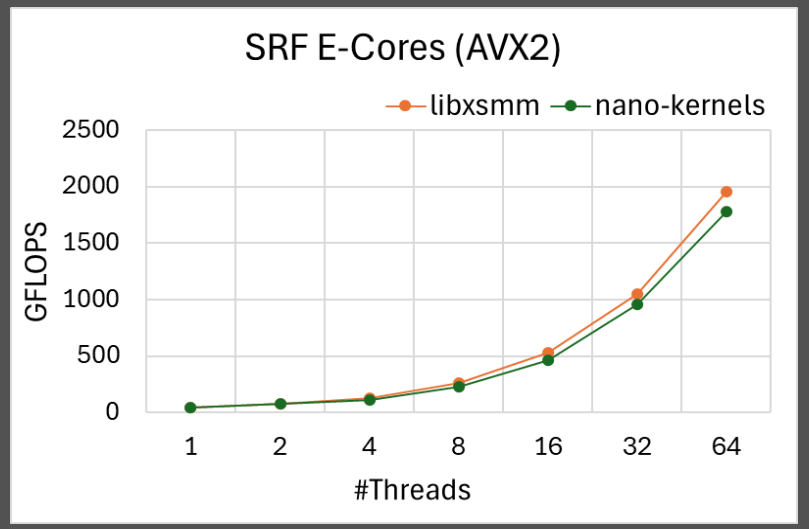
- TPP-MLIR (libxsmm)
  - libxsmm library for microkernels
  - Perf better than Intel oneMKL and oneDNN

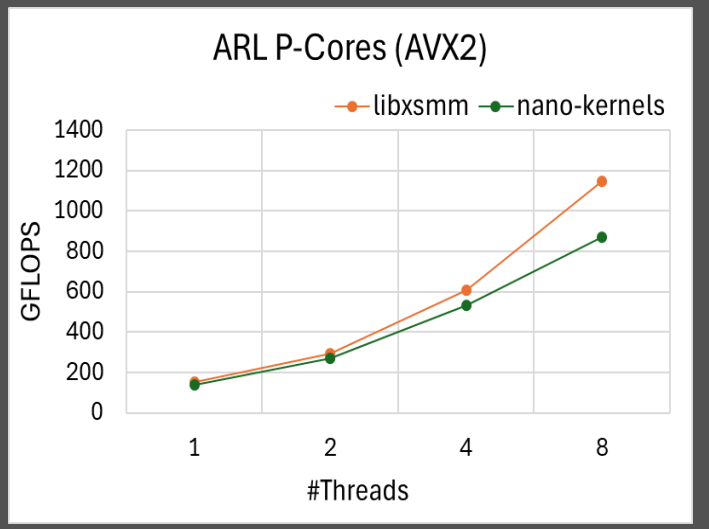
- TPP-MLIR (nanokernels)
  - MLIR target-specific code generation
  - Self-contained, no external libraries

- Methodology
  - Measure only benchmark loop (no init, others…)
  - https://github.com/libxsmm/tpp-mlir/tree/main/benchmarks

Benchmarks – F32



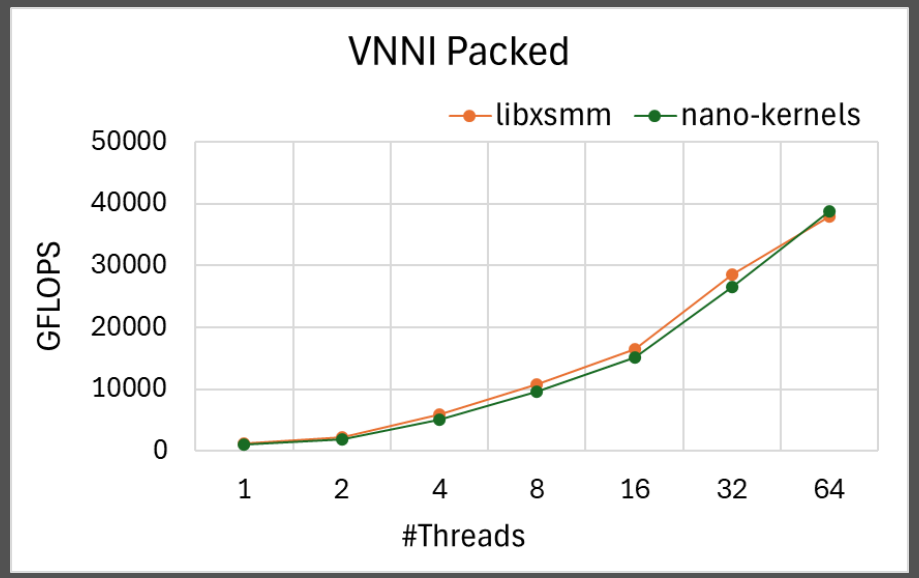


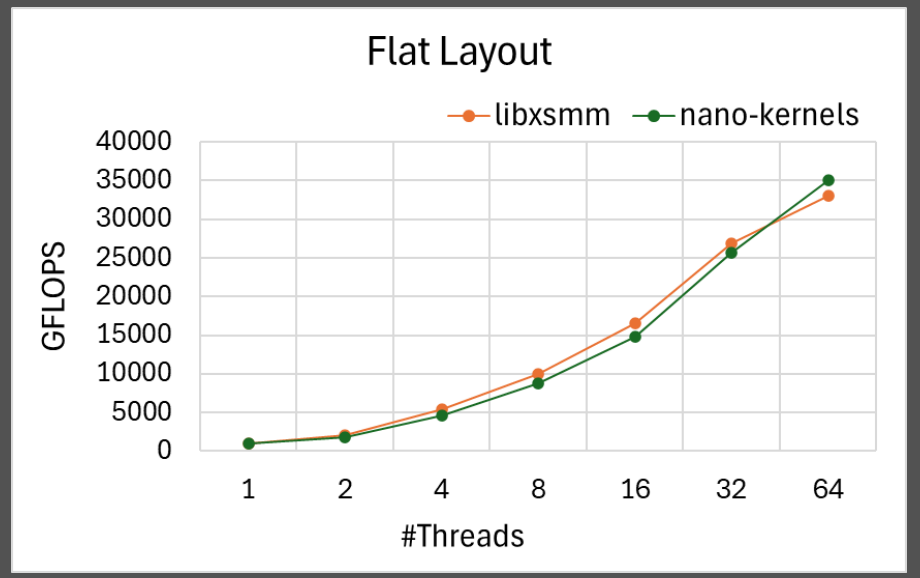


- Register Tile sizes:
  - AVX512 – M:8 N:32 K:1
  - AVX2 - M:4 N:16 K:1

- ~93% and ~91% of libxsmm performance on **EMR** and **SRF**
- **ARL** dip with 8 threads due to **parallelization scheme**

Benchmarks – BF16 AMX (EMR)

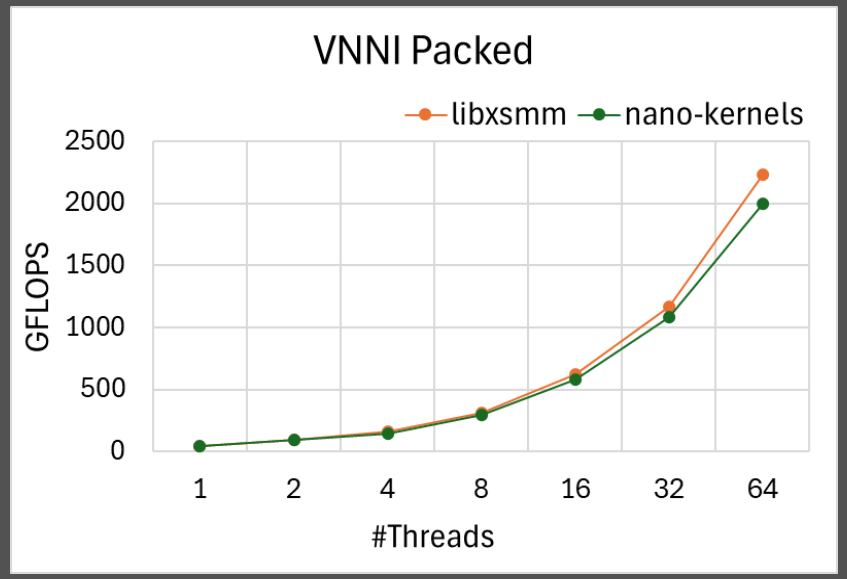


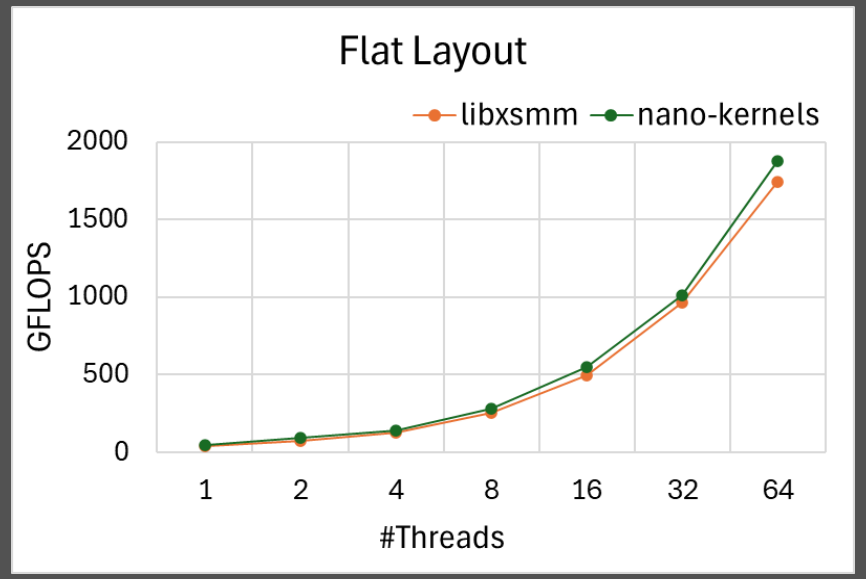


- Register Tile size:
  - M:32 N:32 K:32

- Flat layout input is shuffled to VNNI packed
- ~91% and ~93% libxsmm performance for **VNNI packed** and **Flat** input.

Benchmarks – BF16 AVX2 (SRF E-Cores)





- Register Tile size:
  - M:2 N:32 K:2 (VNNI) K:1(Flat),

- No packing from Flat to VNNI - use of BF16 packed instructions
- Nano-kernels outperform libxsmm by ~15% on Flat inputs – due to libxsmm packing input to VNNI

Try It Yourself!

Lighthouse Example

https://github.com/llvm/lighthouse/blob/main/examples/cpu/x86/matmul.py

Upstreaming

Deeper Dive

White Paper

Thangamani et al.
Library Liberation (2025)
https://arxiv.org/abs/2511.13764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